

## Complementary Trench MOSFET

### 2NP05

#### ■ Features

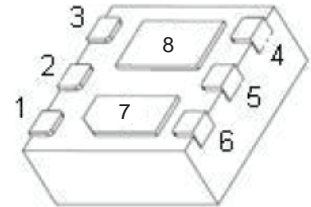
N-Channel

- $V_{DS} (V) = 20V$
- $I_D = 4.5 A (V_{GS} = 4.5V)$
- $R_{DS(ON)} < 29m\Omega (V_{GS} = 4.5V)$
- $R_{DS(ON)} < 34m\Omega (V_{GS} = 2.5V)$
- $R_{DS(ON)} < 44m\Omega (V_{GS} = 1.8V)$
- $R_{DS(ON)} < 65m\Omega (V_{GS} = 1.5V)$

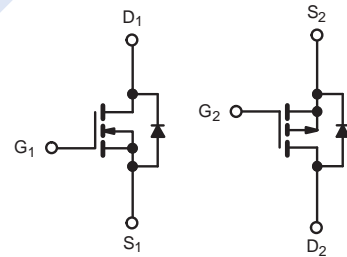
P-Channel

- $V_{DS} (V) = -20V$
- $I_D = -4.5 A (V_{GS} = -4.5V)$
- $R_{DS(ON)} < 61m\Omega (V_{GS} = -4.5V)$
- $R_{DS(ON)} < 81m\Omega (V_{GS} = -2.5V)$
- $R_{DS(ON)} < 115m\Omega (V_{GS} = -1.8V)$
- $R_{DS(ON)} < 170m\Omega (V_{GS} = -1.5V)$

DFN2X2-6



1.S1	5.G2
2.G1	6.D1
3.D2	7.D1
4.S2	8.D2



N-Channel MOSFET P-Channel MOSFET

#### ■ Absolute Maximum Ratings $T_a = 25^\circ C$

Parameter		Symbol	N-Channel	P-Channel	Unit
Drain-Source Voltage		$V_{DS}$	20	-20	V
Gate-Source Voltage		$V_{GS}$	$\pm 8$		
Continuous Drain Current	$T_C=25^\circ C$	$I_D$	4.5	-4.5	A
	$T_C=70^\circ C$		4.5	-4.5	
	$T_A=25^\circ C$		4.5	-4.3	
	$T_A=70^\circ C$		4.5	-3.8	
Pulsed Drain Current		$I_{DM}$	20	-15	
Power Dissipation	$T_C=25^\circ C$	$P_D$	6.5		W
	$T_C=70^\circ C$		5		
	$T_A=25^\circ C$		1.9		
	$T_A=70^\circ C$		1.2		
Thermal Resistance.Junction- to-Ambient	$t \leq 5s$	$R_{thJA}$	65		$^\circ C/W$
Thermal Resistance.Junction- to-Case		$R_{thJC}$	16		
Junction Temperature		$T_J$	150		$^\circ C$
Storage Temperature Range		$T_{stg}$	-55 to 150		

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■ Electrical Characteristics Ta = 25°C

Parameter	Symbol	Test Conditions	Type	Min	Typ	Max	Unit
Drain-Source Breakdown Voltage	V <sub>DSS</sub>	I <sub>D</sub> =250 μA, V <sub>GS</sub> =0V	N-CH	20			V
		I <sub>D</sub> =-250 μA, V <sub>GS</sub> =0V	P-CH	-20			
Zero Gate Voltage Drain Current	I <sub>DSS</sub>	V <sub>DS</sub> =20V, V <sub>GS</sub> =0V	N-CH			1	μA
		V <sub>DS</sub> =-20V, V <sub>GS</sub> =0V	P-CH			-1	
		V <sub>DS</sub> =20V, V <sub>GS</sub> =0V, T <sub>J</sub> =55°C	N-CH			10	
		V <sub>DS</sub> =-20V, V <sub>GS</sub> =0V, T <sub>J</sub> =55°C	P-CH			-10	
Gate-Body Leakage Current	I <sub>GSS</sub>	V <sub>DS</sub> =0V, V <sub>GS</sub> =±8V	N-CH			±100	nA
		V <sub>DS</sub> =0V, V <sub>GS</sub> =±8V	P-CH			±100	
Gate Threshold Voltage	V <sub>GS(th)</sub>	V <sub>DS</sub> =V <sub>GS</sub> , I <sub>D</sub> =250 μA	N-CH	0.4		1	V
		V <sub>DS</sub> =V <sub>GS</sub> , I <sub>D</sub> =-250 μA	P-CH	-0.4		-1	
Static Drain-Source On-Resistance	R <sub>DS(on)</sub>	V <sub>GS</sub> =4.5V, I <sub>D</sub> =5A	N-CH			29	mΩ
		V <sub>GS</sub> =2.5V, I <sub>D</sub> =4.6A				34	
		V <sub>GS</sub> =1.8V, I <sub>D</sub> =4.1A				44	
		V <sub>GS</sub> =1.5V, I <sub>D</sub> =2A				65	
		V <sub>GS</sub> =-4.5V, I <sub>D</sub> =-3.6A	P-CH			61	
		V <sub>GS</sub> =-2.5V, I <sub>D</sub> =-3.2A				81	
		V <sub>GS</sub> =-1.8V, I <sub>D</sub> =-1A				115	
		V <sub>GS</sub> =-1.5V, I <sub>D</sub> =-1A				170	
On-State Drain Current	I <sub>D(on)</sub>	V <sub>DS</sub> ≥5 V, V <sub>GS</sub> = 4.5 V	N-CH	15			A
		V <sub>DS</sub> ≥-5 V, V <sub>GS</sub> = -4.5 V	P-CH	-10			
Forward Transconductance	g <sub>FS</sub>	V <sub>DS</sub> =10V, I <sub>D</sub> =5A	N-CH		21		S
		V <sub>DS</sub> =-10V, I <sub>D</sub> =-3.6A	P-CH		11		
Input Capacitance	C <sub>iss</sub>	N-Channel: V <sub>GS</sub> =0V, V <sub>DS</sub> =6V, f=1MHz	N-CH		500		pF
Output Capacitance	C <sub>oss</sub>		P-Channel: V <sub>GS</sub> =0V, V <sub>DS</sub> =6V, f=1MHz	P-CH		590	
		Reverse Transfer Capacitance	C <sub>rss</sub>	N-Channel: V <sub>GS</sub> =0V, V <sub>DS</sub> =6V, f=1MHz	N-CH		
P-Channel: V <sub>GS</sub> =0V, V <sub>DS</sub> =6V, f=1MHz	P-CH				280		
Gate Resistance	R <sub>g</sub>	V <sub>GS</sub> =0V, f=1MHz	N-CH	0.7		7	Ω
			P-CH	2		20	
Total Gate Charge	Q <sub>g</sub>	V <sub>GS</sub> =8V, V <sub>DS</sub> =6V, I <sub>D</sub> =6.5A	N-CH		9.7	15	nC
		V <sub>GS</sub> =-8V, V <sub>DS</sub> =-6V, I <sub>D</sub> =-4.5A	P-CH		13.1	20	
		N-Channel: V <sub>GS</sub> =4.5V, V <sub>DS</sub> =6V, I <sub>D</sub> =6.5A	N-CH		5.6	8.5	
			P-CH		8.2	12.5	
Gate Source Charge	Q <sub>gs</sub>	V <sub>GS</sub> =4.5V, V <sub>DS</sub> =6V, I <sub>D</sub> =6.5A	N-CH		0.72		
			P-Channel: V <sub>GS</sub> =-4.5V, V <sub>DS</sub> =-6V, I <sub>D</sub> =-4.3A	P-CH		1.2	
Gate Drain Charge	Q <sub>gd</sub>	V <sub>GS</sub> =-4.5V, V <sub>DS</sub> =-6V, I <sub>D</sub> =-4.3A	N-CH		0.74		
			P-CH		2.8		

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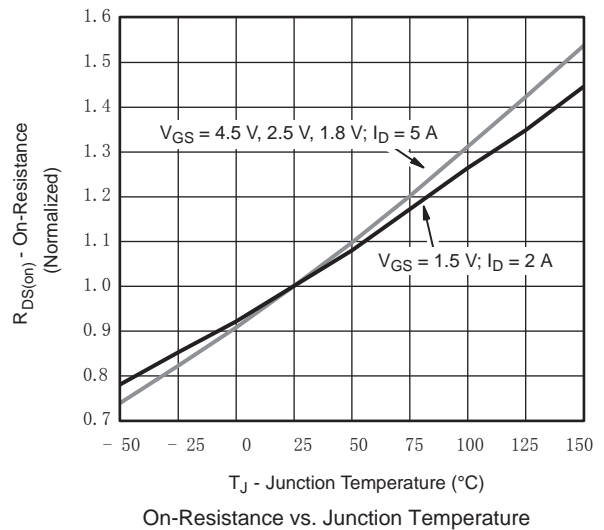
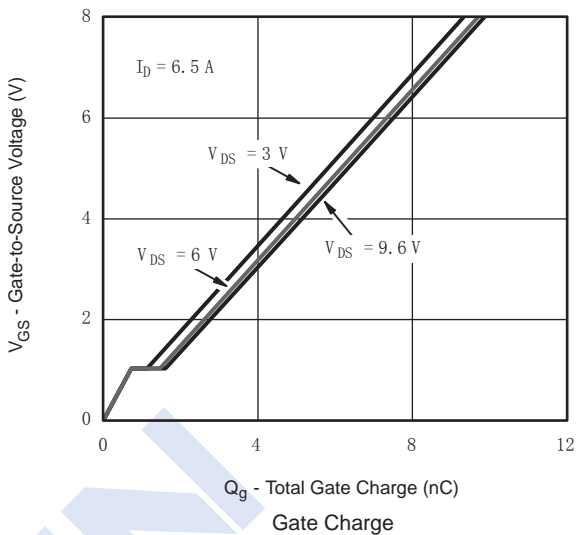
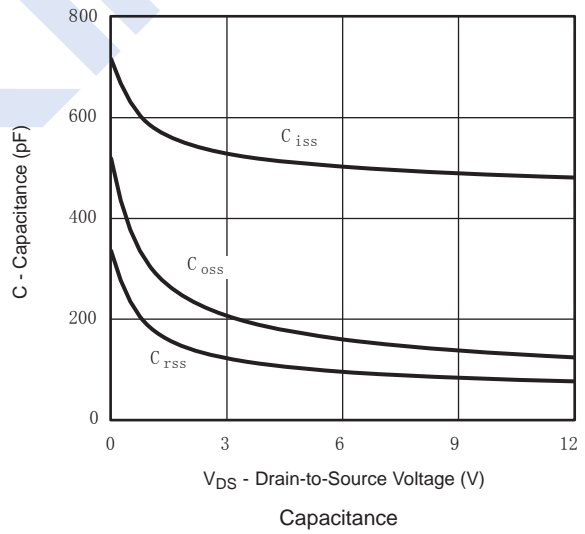
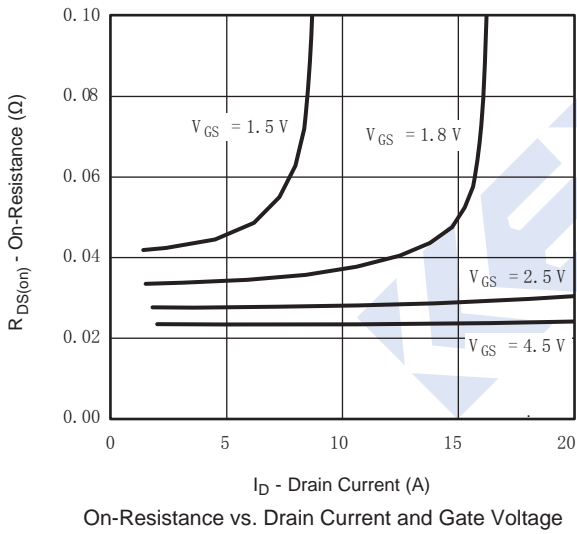
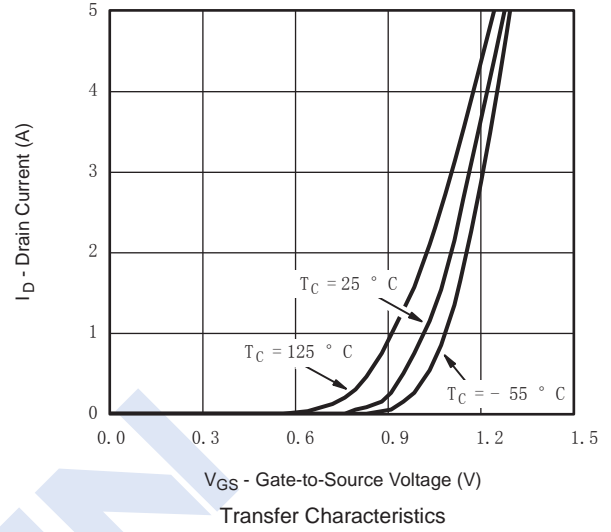
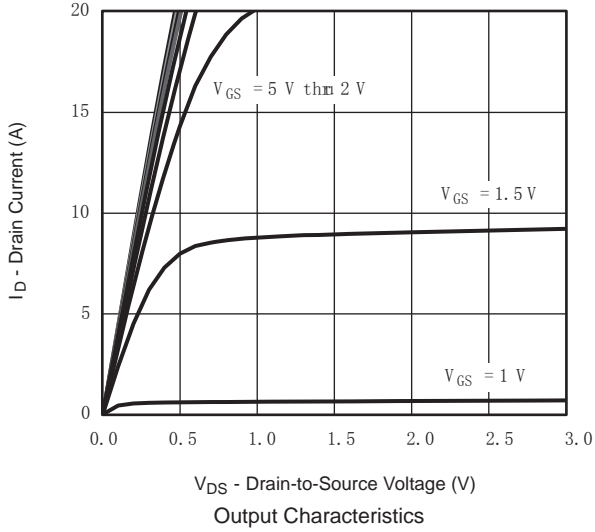
#### ■ Electrical Characteristics Ta = 25°C

Turn-On DelayTime	$t_{d(on)}$	N-Channel: $V_{GS}=4.5V, V_{DS}=6V, I_D=5.2A,$ $R_L=1.2\Omega, R_{GEN}=1\Omega$	N-CH	10	15	ns
			P-CH	30	40	
Turn-On Rise Time	$t_r$	P-Channel: $V_{GS}=-4.5V, V_{DS}=-6V, I_D=-3.8A,$ $R_L=1.6\Omega, R_{GEN}=1\Omega$	N-CH	10	15	
			P-CH	25	40	
Turn-Off DelayTime	$t_{d(off)}$		N-CH	22	30	
			P-CH	30	45	
Turn-Off Fall Time	$t_f$		N-CH	10	15	
			P-CH	20	30	
Turn-On DelayTime	$t_{d(on)}$	N-Channel: $V_{GS}=10V, V_{DS}=6V, I_D=5.2A,$ $R_L=1.2\Omega, R_{GEN}=1\Omega$	N-CH	5	10	ns
			P-CH	8	15	
Turn-On Rise Time	$t_r$	P-Channel: $V_{GS}=-10V, V_{DS}=-6V, I_D=-3.8A,$ $R_L=1.6\Omega, R_{GEN}=1\Omega$	N-CH	10	15	
			P-CH	12	20	
Turn-Off DelayTime	$t_{d(off)}$		N-CH	18	30	
			P-CH	25	40	
Turn-Off Fall Time	$t_f$		N-CH	10	15	
			P-CH	18	30	
Body Diode Reverse Recovery Time	$t_{rr}$	N-Channel $I_F=5.2A, di/dt = 100A/\mu s, T_J = 25^\circ C$ P-Channel $I_F=-3.8A, di/dt = -100 A/\mu s, T_J = 25^\circ C$	N-CH	20	40	nS
			P-CH	30	60	
Body Diode Reverse Recovery Charge	$Q_{rr}$		N-CH	5	10	nC
			P-CH	12	24	
Reverse Recovery Fall Time	$t_a$		N-CH	8		nS
			P-CH	16		
Reverse Recovery Rise Time	$t_b$		N-CH	12		nS
			P-CH	14		
Maximum Body-Diode Continuous Current	$I_S$	$T_c = 25^\circ C$	N-CH		4.5	A
			P-CH		-4.5	
Pulsed Body-Diode Current *	$I_{SM}$		N-CH		20	A
			P-CH		-10	
Diode Forward Voltage	$V_{SD}$	$I_S=5.2A, V_{GS}=0V$	N-CH		1.2	V
		$I_S=-3.4A, V_{GS}=0V$	P-CH		-1.2	

Note. Pulse test; pulse width  $\leq 300 \mu s$ , duty cycle  $\leq 2\%$ .

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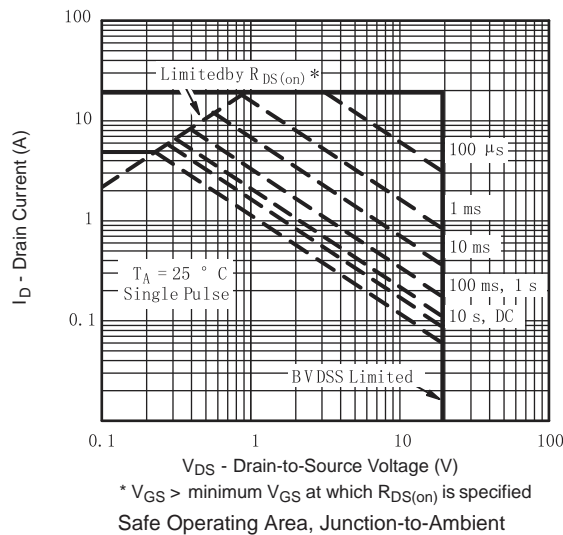
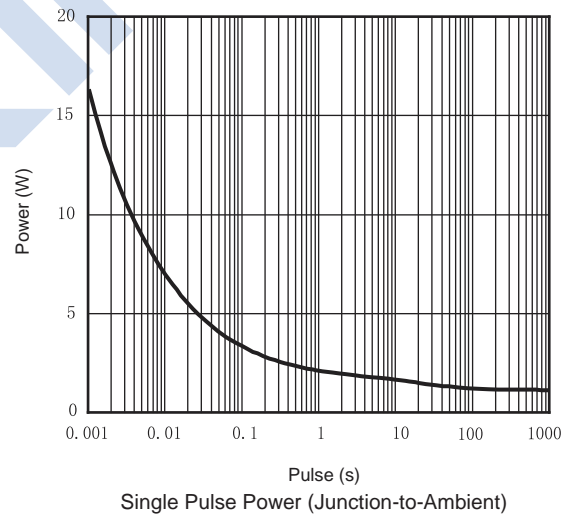
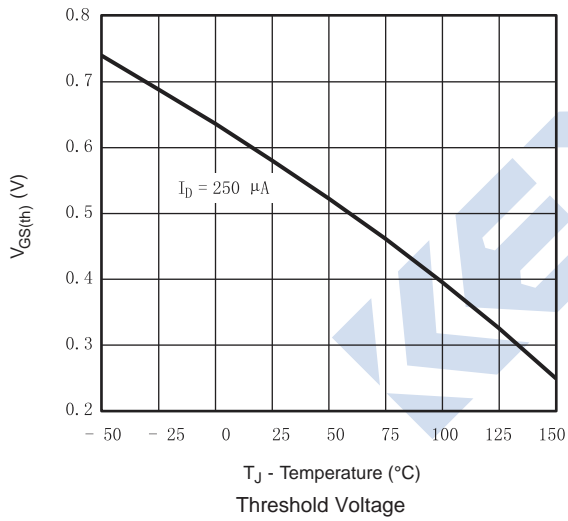
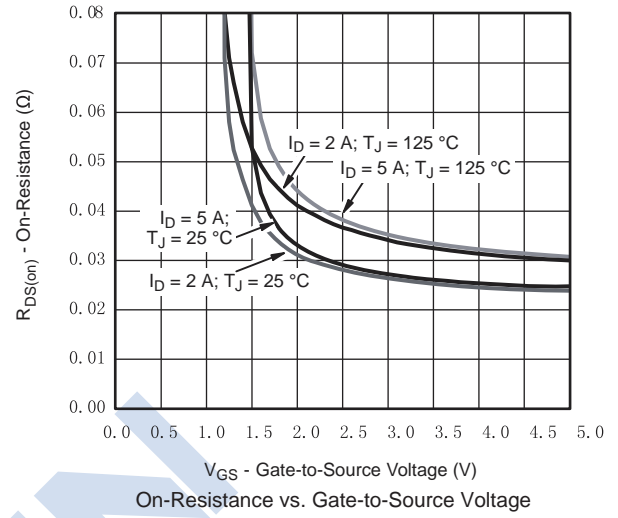
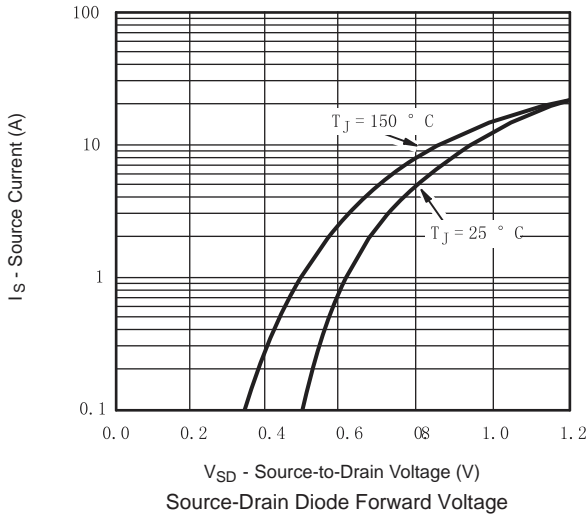
### ■ N-Channel Typical Characteristics



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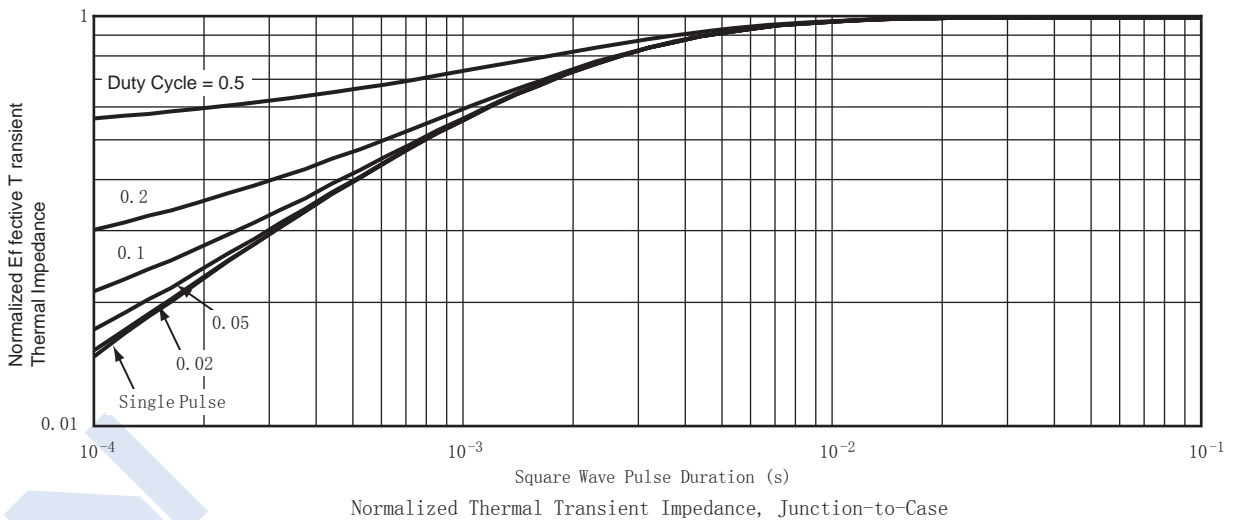
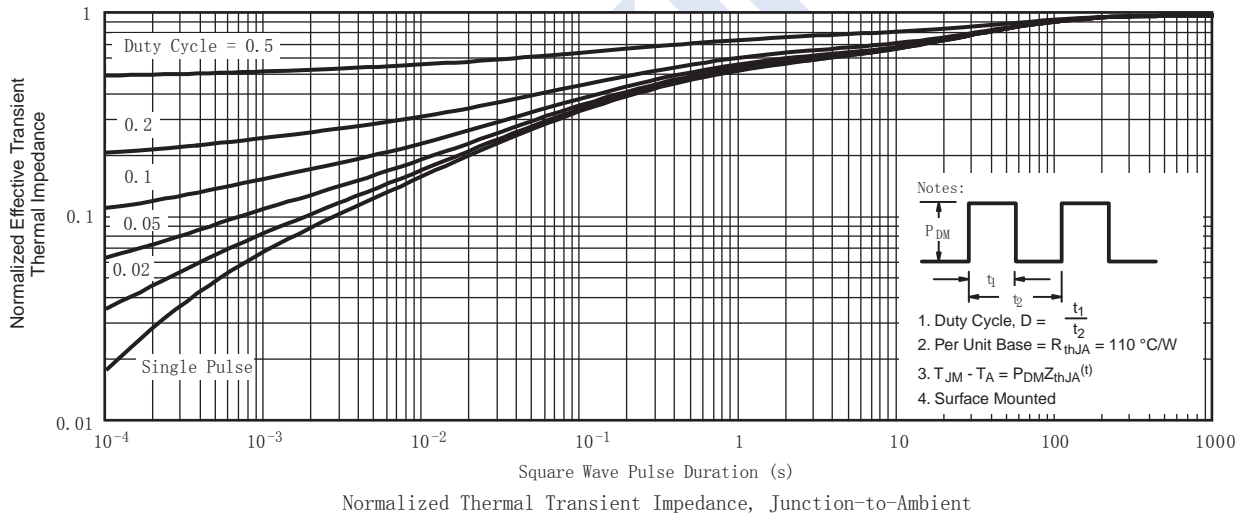
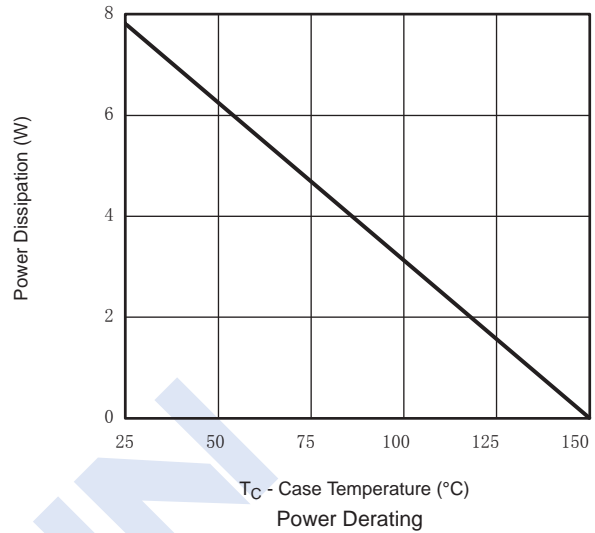
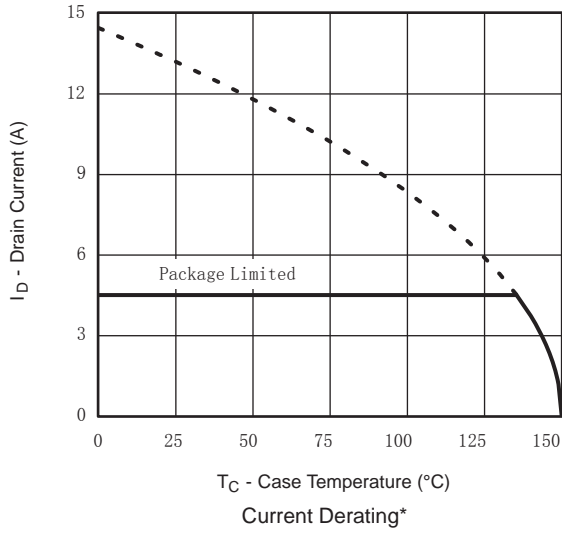
### ■ N-Channel Typical Characteristics



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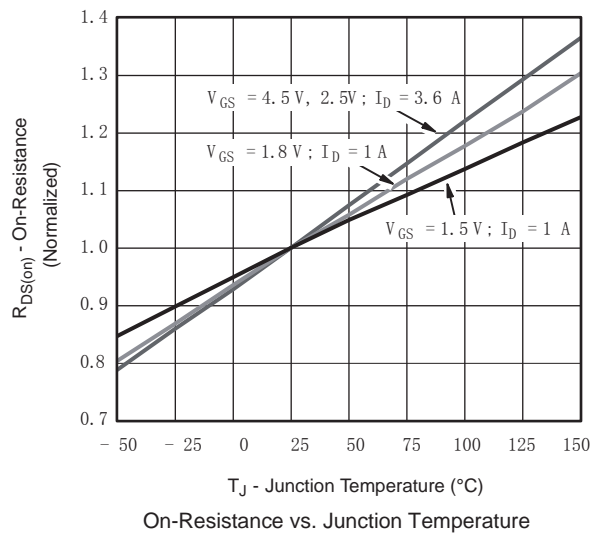
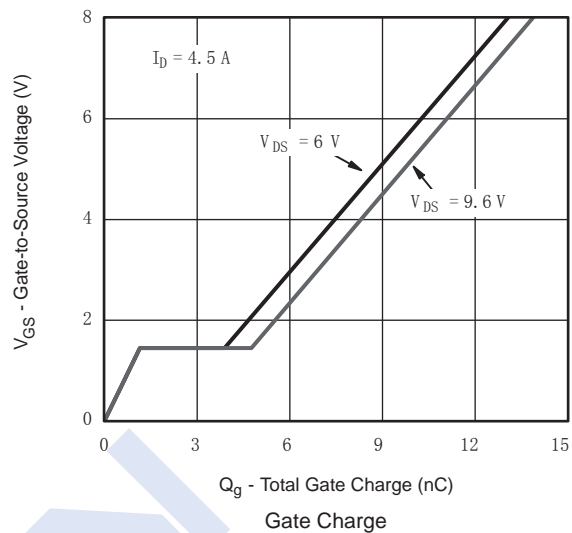
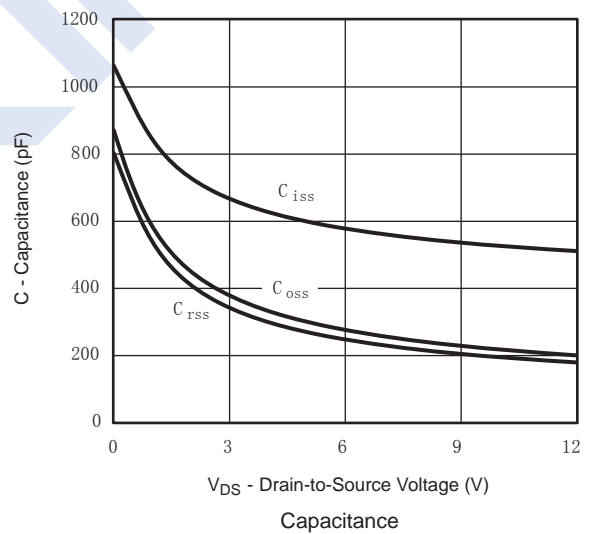
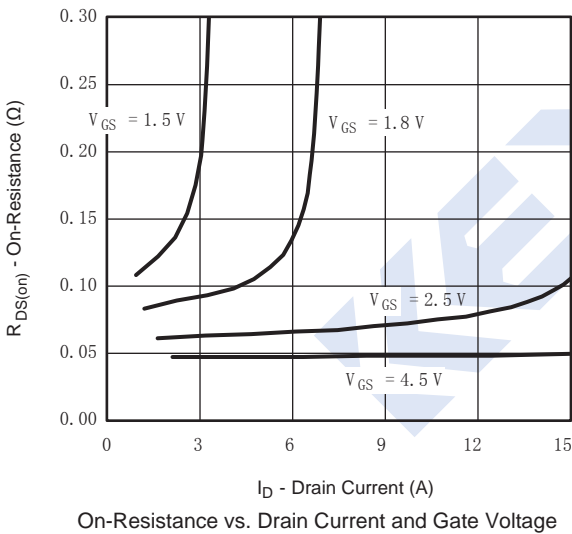
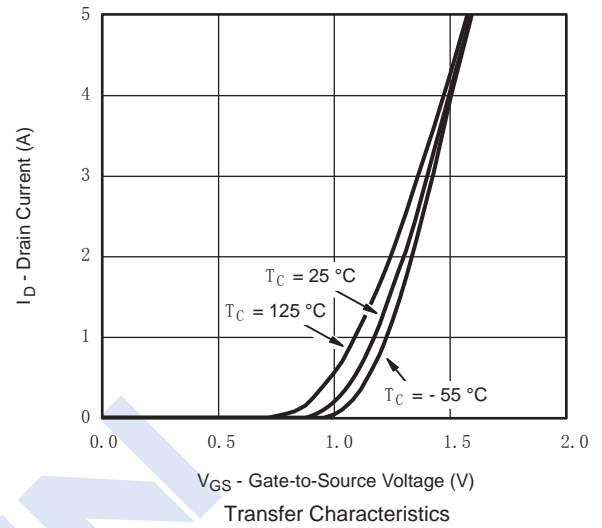
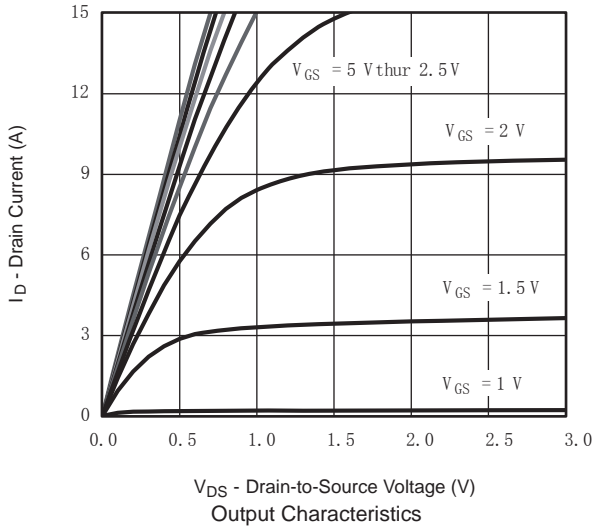
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### ■ N-Channel Typical Characteristics



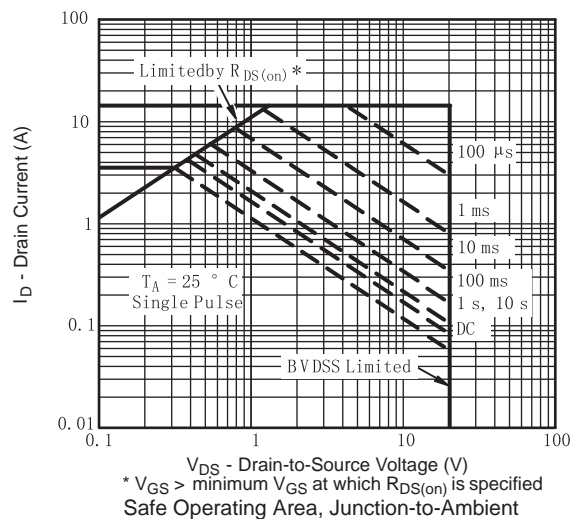
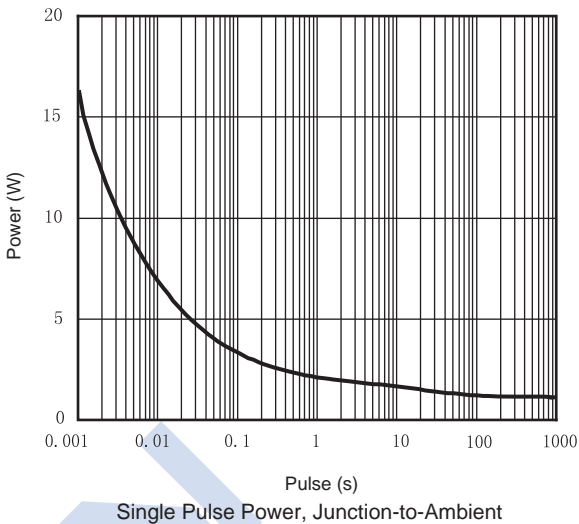
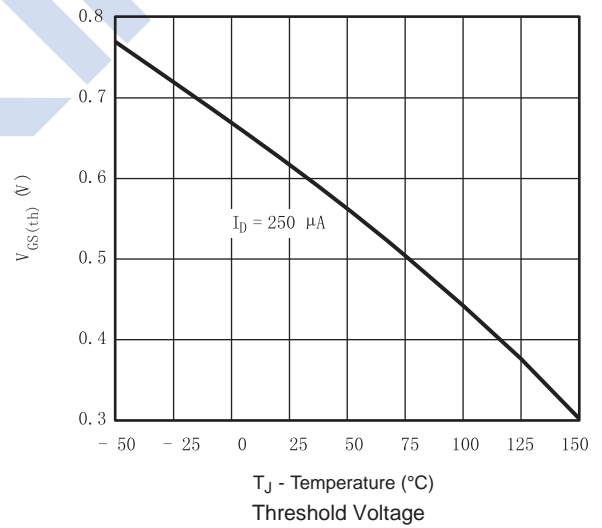
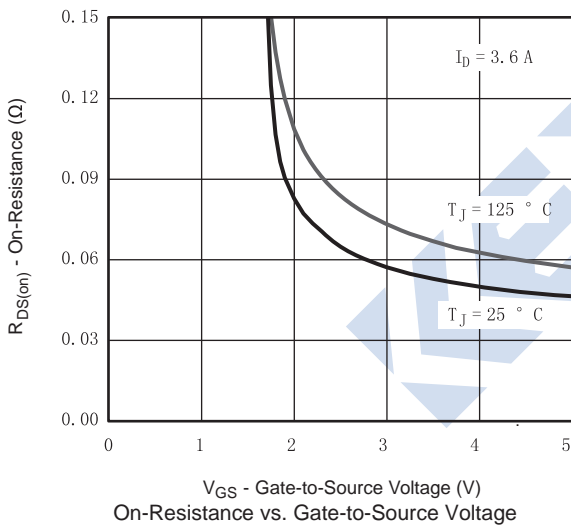
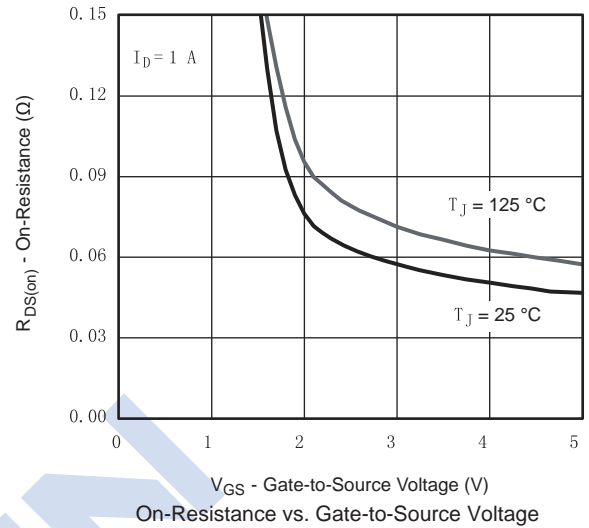
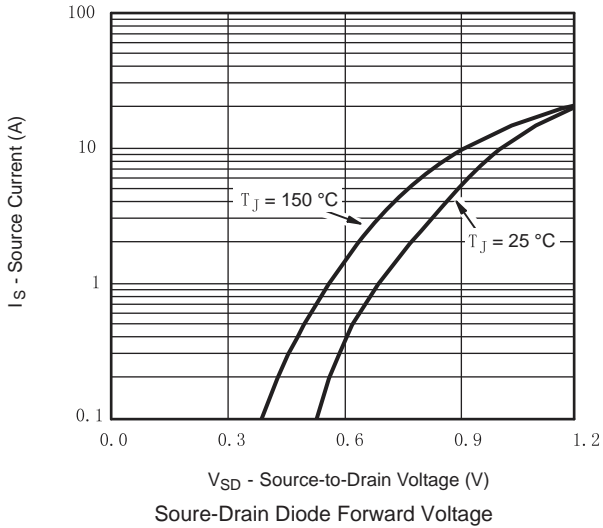
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### ■ P-Channel Typical Characteristics



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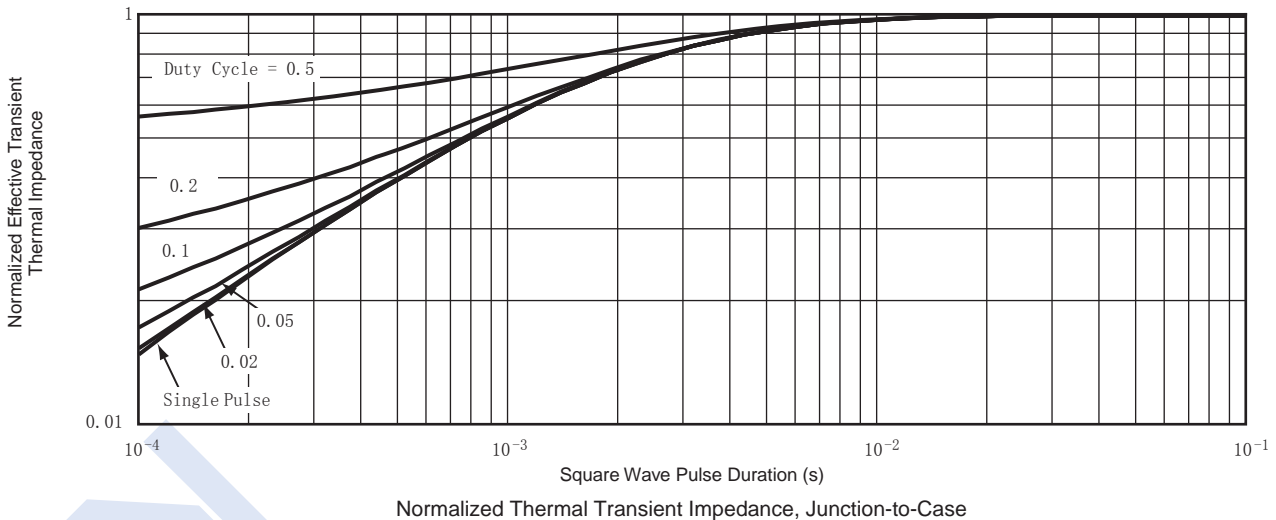
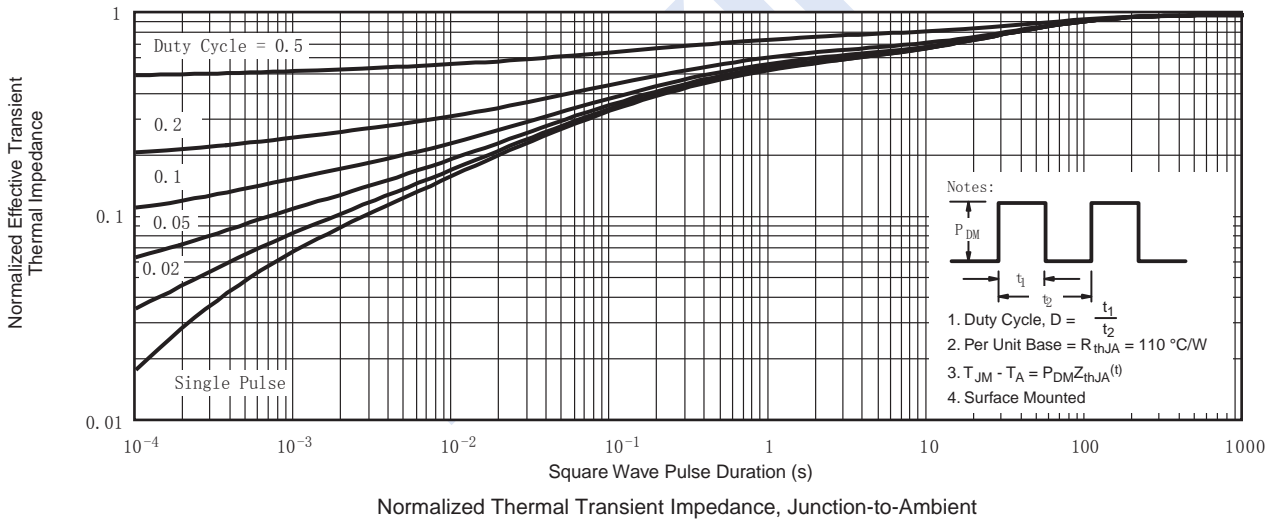
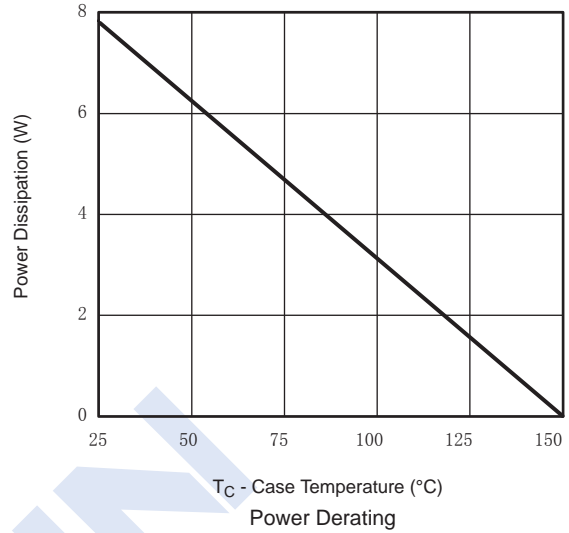
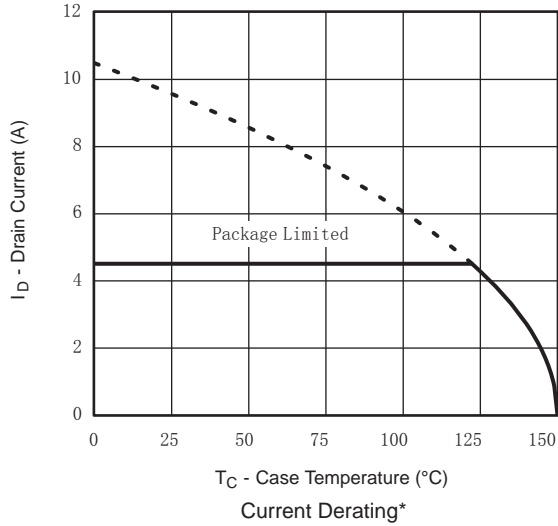
### ■ P-Channel Typical Characteristics





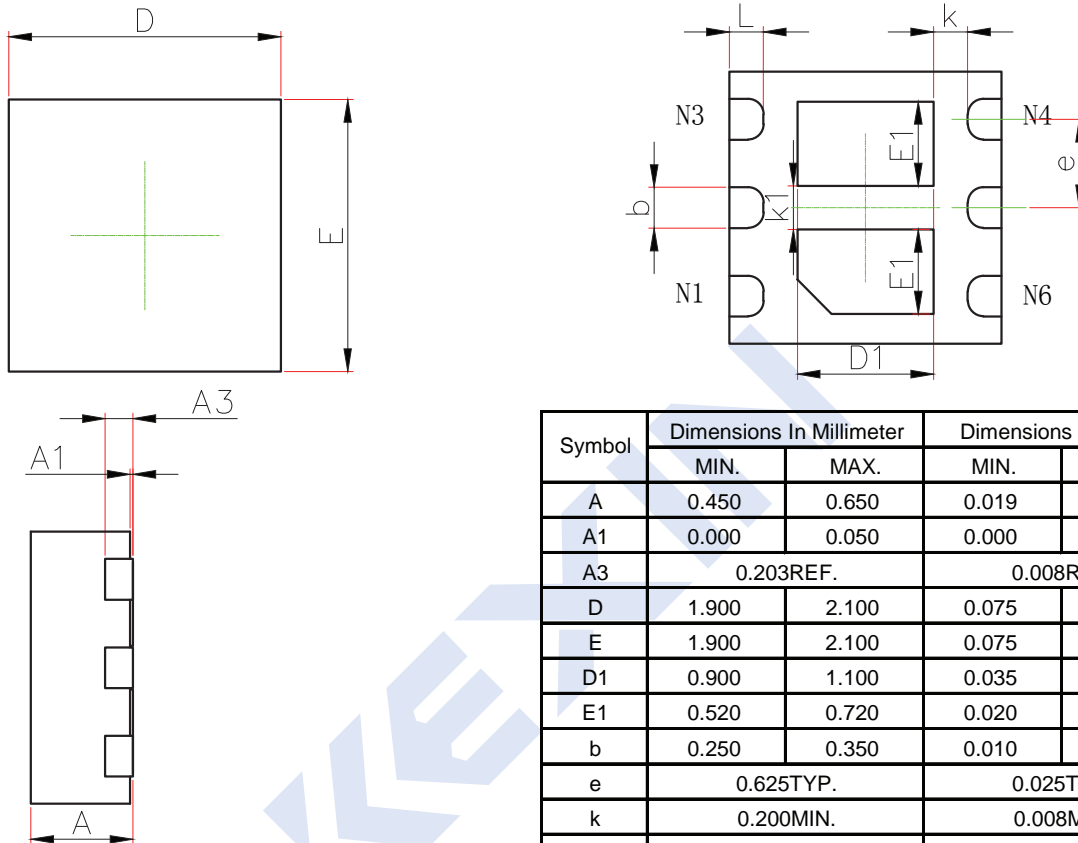
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■ P-Channel Typical Characteristics

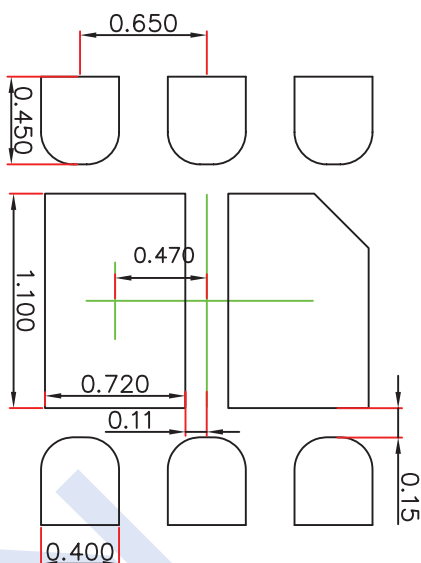


## Complementary Trench MOSFET 2NP05

### DFN2X2-6 Package Outline Dimensions



### Suggested Pad Layout



#### Note:

1. Controlling dimension: in millimeters,
2. General tolerance:  $\pm 0.050\text{mm}$ ,
3. The pad layout is for reference purposes only.