

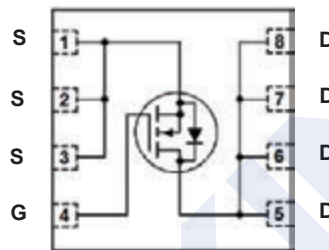
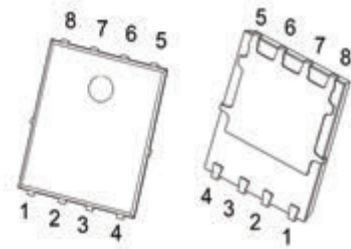
## N-Channel MOSFET

## 2KK5074DFN

## ■ Features

- $V_{DS} = 40\text{ V}$
- $I_D = 150\text{ A}$
- $R_{DS(ON)} < 2.4\text{ m}\Omega @ V_{GS}=10\text{V}$
- $R_{DS(ON)} < 3.5\text{ m}\Omega @ V_{GS}=4.5\text{V}$
- 100% UIS Tested
- 100% Rg Tested

PDFN5x6-8

■ Absolute Maximum Ratings ( $T_A = 25^\circ\text{C}$  unless otherwise noted)

Parameter	Symbol	Rating	Unit
Drain-Source Voltage	$V_{DS}$	40	V
Gate-Source Voltage	$V_{GS}$	$\pm 20$	
Continuous Drain Current (Note 1)	$I_D$	150	A
Pulsed Drain Current (Note 2)	$I_{DM}$	450	
Avalanche Energy (Note 2)	$E_{AS}$	163	mJ
Power Dissipation (Note 3)	$P_D$	78	
	$P_D$	31	
Thermal Resistance, Junction- to-Ambient	$R_{\theta JA}$	50	$^\circ\text{C}/\text{W}$
Thermal Resistance, Junction- to-Case	$R_{\theta JC}$	1.6	
Junction and Storage Temperature Range	$T_{stg}$	-55 to 150	$^\circ\text{C}$

Notes:

1. The maximum current rating is package limited.
2. Repetitive rating; pulse width limited by max. junction temperature.
3.  $P_D$  is based on max. junction temperature, using junction-case thermal resistance.

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■ Electrical Characteristics (T<sub>J</sub> = 25°C unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
<b>Static Parameter</b>						
Drain-Source Breakdown Voltage	BV <sub>DSS</sub>	I <sub>D</sub> = 250 μA, V <sub>GS</sub> = 0V	40			V
Zero Gate Voltage Drain Current	I <sub>DSS</sub>	V <sub>DS</sub> = 40 V, V <sub>GS</sub> = 0 V			1	μA
		V <sub>DS</sub> = 40 V, V <sub>GS</sub> = 0 V, T <sub>J</sub> = 55°C			5	
Gate to Source Leakage Current	I <sub>GSS</sub>	V <sub>DS</sub> = 0 V, V <sub>GS</sub> = ±20 V			±100	nA
Gate to Source Threshold Voltage	V <sub>GS(th)</sub>	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = 250μA	1.0		2.4	V
Static Drain-Source On-Resistance	R <sub>DS(on)</sub>	V <sub>GS</sub> = 10 V, I <sub>D</sub> = 20 A		1.6	2.4	mΩ
		V <sub>GS</sub> = 4.5 V, I <sub>D</sub> = 20 A			3.5	
Forward Transconductance	g <sub>FS</sub>	V <sub>DS</sub> =5V, I <sub>D</sub> =20A		100		S
<b>Dynamic Parameters</b>						
Input Capacitance	C <sub>iss</sub>	V <sub>GS</sub> = 0 V, V <sub>DS</sub> = 20 V, f = 1MHz		1760		pF
Output Capacitance	C <sub>oss</sub>			675		
Reverse Transfer Capacitance	C <sub>rss</sub>			60		
Gate Resistance	R <sub>g</sub>	f=1MHz, Open drain	0.3	0.7	1.1	Ω
<b>Switching Parameters</b>						
Total Gate Charge	Q <sub>g</sub>	V <sub>GS</sub> = 10V, V <sub>DS</sub> = 20 V, I <sub>D</sub> = 20 A		50	70	nC
Gate Source Charge	Q <sub>gs</sub>			11.5		
Gate Drain Charge	Q <sub>gd</sub>			4		
Turn-On Delay Time	t <sub>d(on)</sub>	V <sub>GS</sub> = 10V, V <sub>DD</sub> = 20 V, R <sub>L</sub> =1.0 Ω, R <sub>GEN</sub> = 3.0 Ω		11		ns
Turn-On Rise Time	t <sub>r</sub>			3.5		
Turn-Off Delay Time	t <sub>d(off)</sub>			36		
Turn-Off Fall Time	t <sub>f</sub>			3		
<b>Drain-Source Diode Characteristics</b>						
Reverse Recovery Charge	Q <sub>rr</sub>	I <sub>F</sub> =20A, di/dt=500A/μs		45		nC
Reverse Recovery Time	t <sub>rr</sub>			17		ns
Maximum Body-Diode Continuous Current	I <sub>S</sub>				130	A
Diode Forward Voltage	V <sub>SD</sub>	V <sub>GS</sub> = 0 V, I <sub>S</sub> = 20 A			1.3	V

## Notes:

- The static characteristics in Figures 1 to 6 are obtained using <300μs pulses, duty cycle 0.5% max.
- These curves are based on the junction-to-case thermal impedance which is measured with the device mounted to a large heatsink, assuming a maximum junction temperature of T<sub>J(MAX)</sub>=150°C. The SOA curve provides a single pulse rating.
- These tests are performed with the device mounted on 1 in<sup>2</sup> FR-4 board with 2oz. Copper, in a still air environment with T<sub>A</sub>=25°C.

## ■ Marking

Marking	K5074 KC***
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# N-Channel MOSFET

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### Typical Electrical and Thermal Characteristics

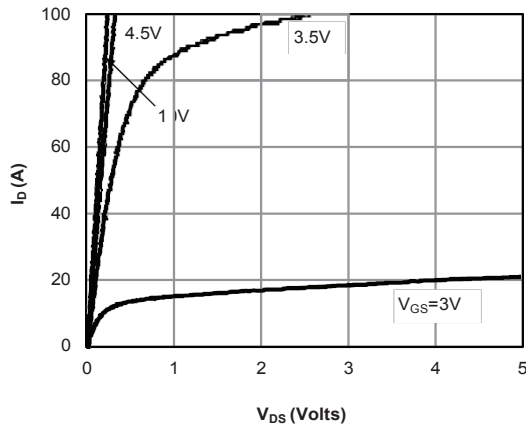


Figure 1: On-Region Characteristics (NOTE 4)

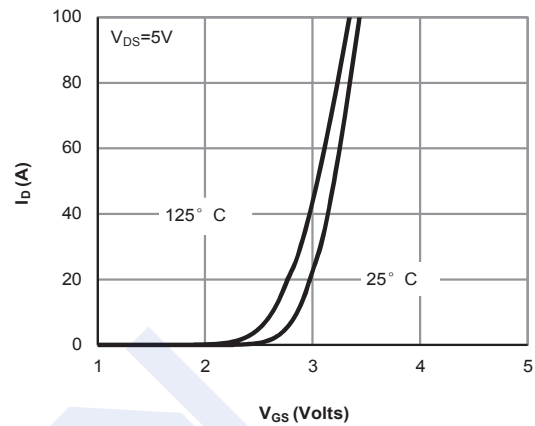


Figure 2: Transfer Characteristics (NOTE 4)

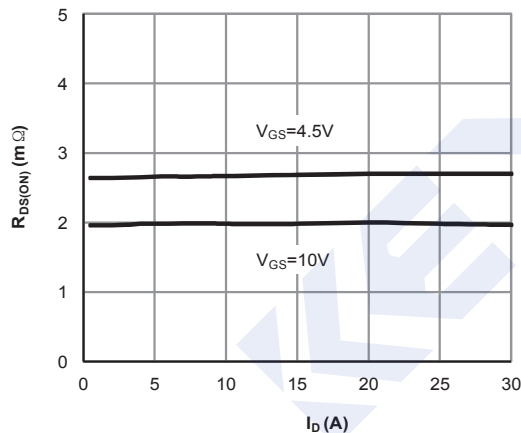


Figure 3: On-Resistance vs. Drain Current and Gate Voltage (NOTE 4)

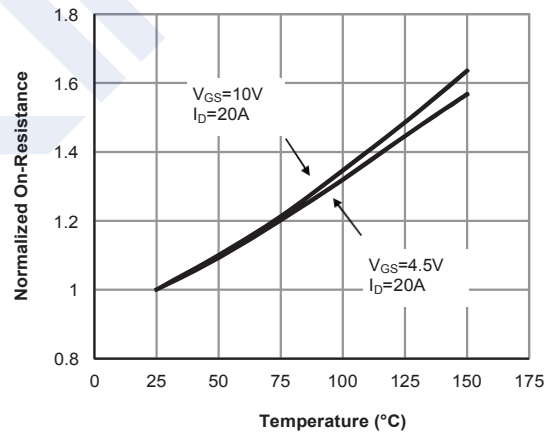


Figure 4: On-Resistance vs. Junction Temperature (NOTE 4)

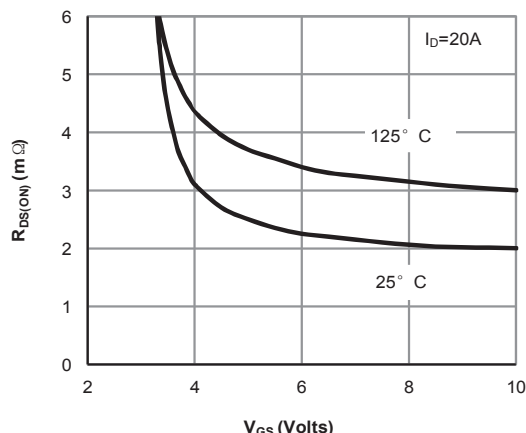


Figure 5: On-Resistance vs. Gate-Source Voltage (NOTE 4)

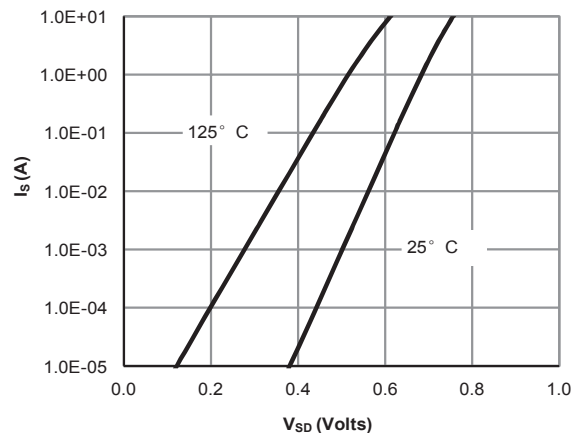


Figure 6: Body-Diode Characteristics (NOTE 4)

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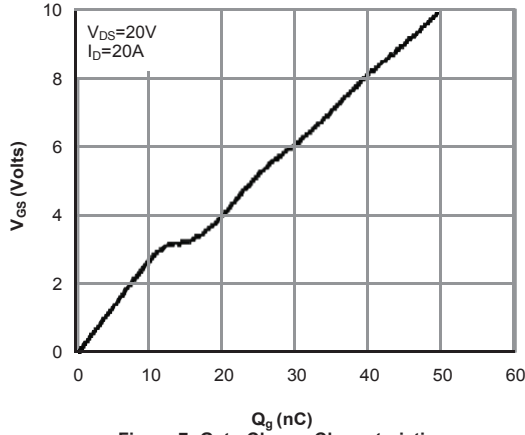


Figure 7: Gate-Charge Characteristics

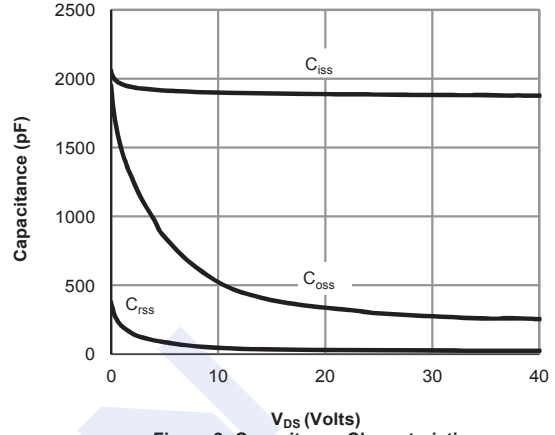


Figure 8: Capacitance Characteristics

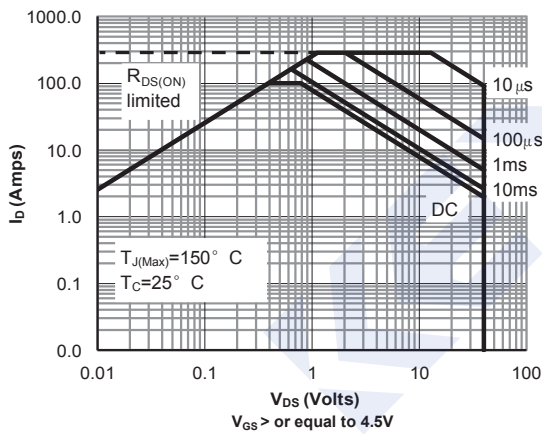


Figure 9: Maximum Forward Biased Safe Operating Area (NOTE 5)

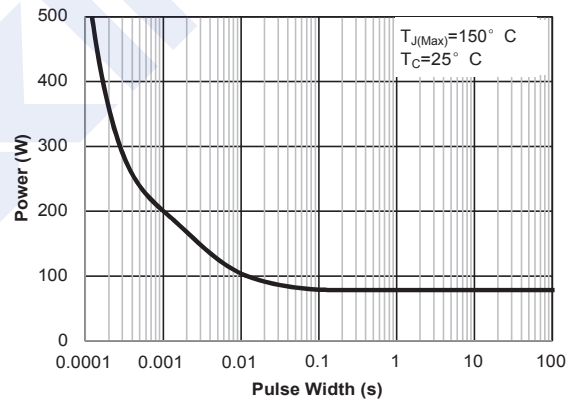


Figure 10: Single Pulse Power Rating Junction-to-Case (NOTE 5)

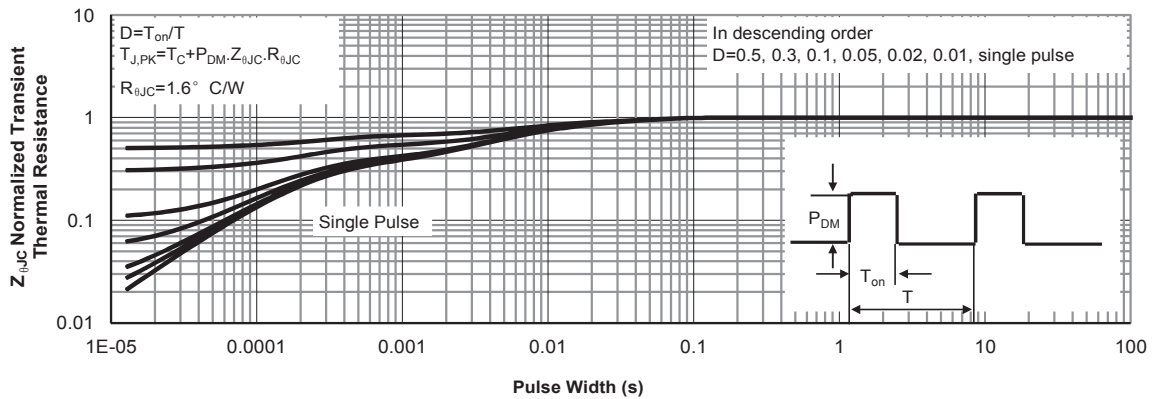


Figure 11: Normalized Maximum Transient Thermal Impedance (NOTE 5)

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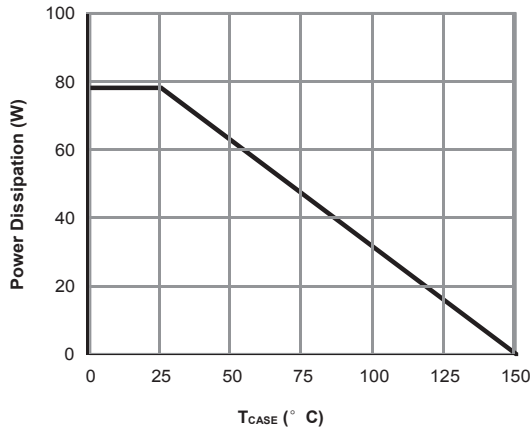


Figure 12: Power De-rating (NOTE 5)

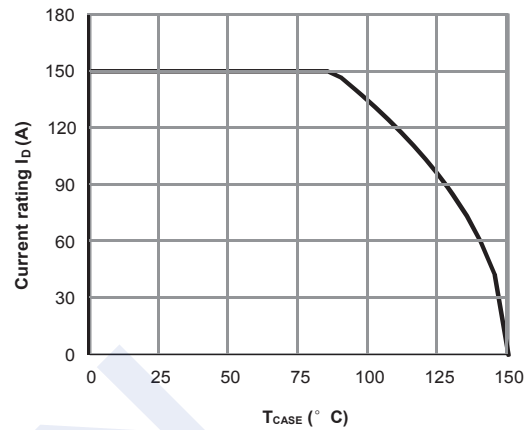


Figure 13: Current De-rating (NOTE 5)

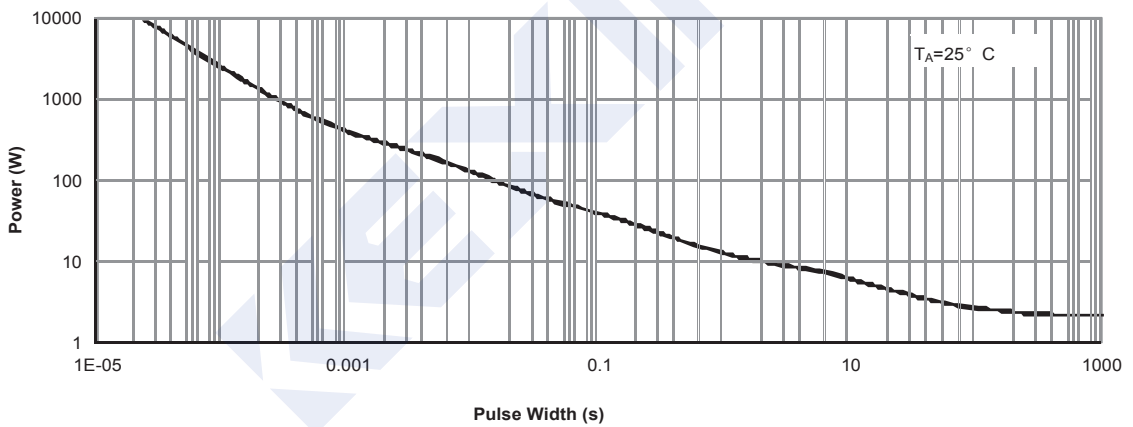


Figure 14: Single Pulse Power Rating Junction-to-Ambient (NOTE 6)

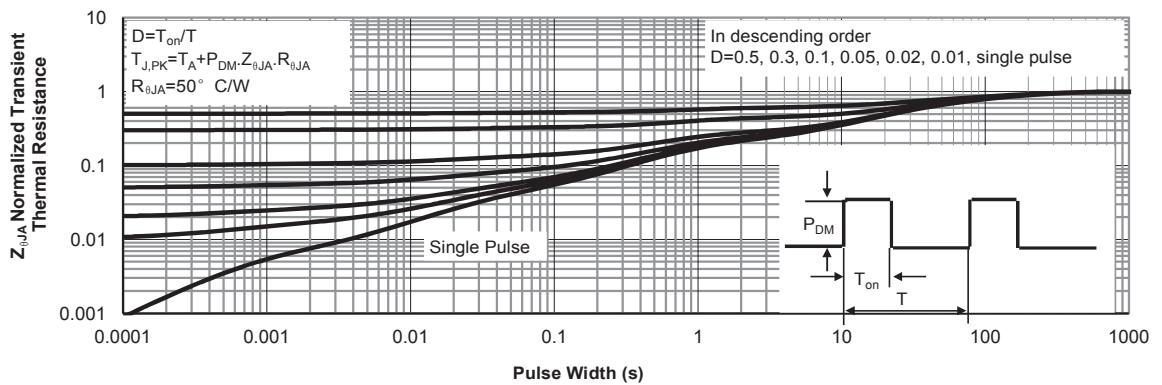
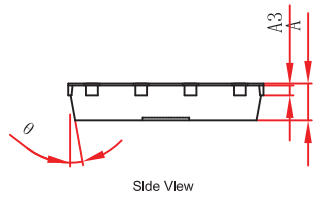
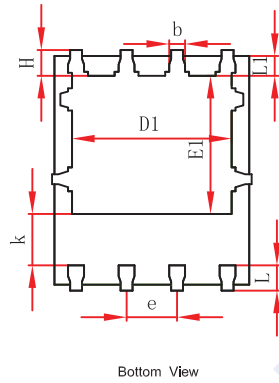
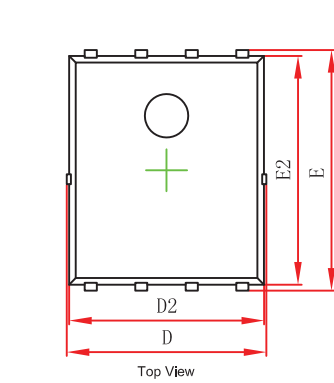


Figure 15: Normalized Maximum Transient Thermal Impedance (NOTE 6)

## N-Channel MOSFET

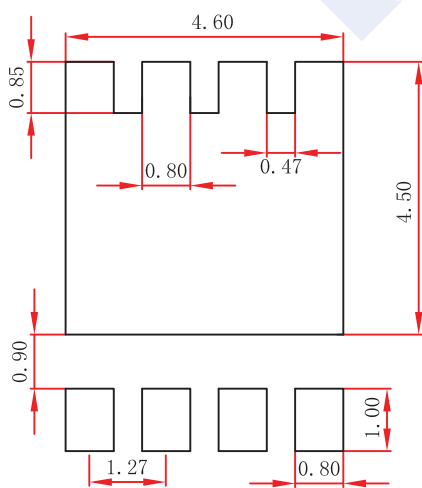
### 2KK5074DFN

#### PDFN5x6-8 Package Outline Dimensions



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	0.900	1.000	0.035	0.039
A3	0.254REF.		0.010REF.	
D	4.944	5.096	0.195	0.201
E	5.974	6.126	0.235	0.241
D1	3.910	4.110	0.154	0.162
E1	3.375	3.575	0.133	0.141
D2	4.824	4.976	0.190	0.196
E2	5.674	5.826	0.223	0.229
k	1.190	1.390	0.047	0.055
b	0.350	0.450	0.014	0.018
e	1.270TYP.		0.050TYP.	
L	0.559	0.711	0.022	0.028
L1	0.424	0.576	0.017	0.023
H	0.574	0.726	0.023	0.029
θ	10°	12°	10°	12°

#### PDFN5x6-8 Suggested Pad Layout



Note:  
 1. Controlling dimension: in millimeters.  
 2. General tolerance: ±0.05mm.  
 3. The pad layout is for reference purposes only.